

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	676	703/1.ccls.	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/09/18 16:10
L2	117	706/919.ccls.	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/09/18 16:20
L3	155	715/964.ccls.	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/09/18 16:31
L4	6404	(wire or cable) near rout\$3	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/09/18 16:31
L5	3179	L4 and (clamp or support)	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/09/18 16:32
L6	104	L5 and Cad	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/09/18 16:42
L7	317	((wir\$3 or cabl\$3) near route) and (cad or cae or (computer adj aided))	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/09/18 16:54
L8	31	((wir\$3 or cabl\$3) near (clamp or fastener)) and (cad or cae or (computer adj aided))	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/09/18 17:25
L9	2	"5021968".pn.	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/09/18 17:23
L10	15	("5021968").URPN.	USPAT	OR	OFF	2005/09/18 17:23
L11	12	((wir\$3 or cabl\$3) near (hanger\$1)) and (cad or cae or (computer adj aided))	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/09/18 17:26



Welcome United States Patent and Trademark Office

☐ Search Results

BROWSE

SEARCH

IEEE XPLORE GUIDE

Results for "'((wire rout*<or>cable rout*)<and>cae) <and> (pyr >= 1951 <and> pyr <= ...)"

Your search matched 4 of 1235066 documents.



A maximum of 500 results are displayed, 100 to a page, sorted by Relevance in Descending order.

» Search Options

[View Session History](#)[New Search](#)

Modify Search

((wire rout*<or>cable rout*)<and>cae) <and> (pyr >= 1951 <and> pyr <= 2001)

☐ Check to search only within this results setDisplay Format: ☒ Citation ☐ Citation & Abstract

» Key

IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

Select Article Information

- ☐ 1. Automatic placement and routing techniques for gate array and standard
Brady, H.N.; Blanks, J.;
Proceedings of the IEEE
Volume 75, Issue 6, June 1987 Page(s):797 - 806
[AbstractPlus](#) | Full Text: [PDF](#)(1015 KB) IEEE JNL
- ☐ 2. A third-generation SPARC V9 64-b microprocessor
Heald, R.; Aingaran, K.; Amir, C.; Ang, M.; Boland, M.; Dixit, P.; Gouldsberry, C.
Grinberg, J.; Hart, J.; Horel, T.; Wen-Jay Hsu; Kaku, J.; Chin Kim; Song Kim; K.
H.; Lauterbach, G.; Lo, R.; McIntyre, H.; Mehta, A.; Murata, D.; Nguyen, S.; Ye
S.; Shin, K.; Tam, K.; Vishwanthaiah, S.; Wu, J.; Yee, G.; You, E.;
Solid-State Circuits, IEEE Journal of
Volume 35, Issue 11, Nov. 2000 Page(s):1526 - 1538
Digital Object Identifier 10.1109/4.881196
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(324 KB) IEEE JNL
- ☐ 3. IEEE recommended practice for industrial and commercial power system
IEEE Std 399-1997
1998
[AbstractPlus](#) | Full Text: [PDF](#)(5712 KB) IEEE STD
- ☐ 4. IEEE standard for integrated circuit (IC) delay and power calculation syst
IEEE Std 1481-1999
26 June 1999 Page(s):i - 390
[AbstractPlus](#) | Full Text: [PDF](#)(1780 KB) IEEE STD

Indexed by
 Inspec[Help](#) [Contact Us](#) [Privacy &](#)

© Copyright 2005 IEEE -



Welcome United States Patent and Trademark Office

☐ Search Results

BROWSE

SEARCH

IEEE XPLORE GUIDE

Results for "((wire rout*<or>cable rout*)<and>cad) <and> (pyr >= 1951 <and> pyr <= ...)"

☐ e-mail

Your search matched 116 of 1235066 documents.

A maximum of 500 results are displayed, 25 to a page, sorted by Relevance in Descending order.

» Search Options

[View Session History](#)
[New Search](#)

Modify Search


☐ Check to search only within this results set
Display Format: ☒ Citation ☐ Citation & Abstract

» Key

IEEE JNL IEEE Journal or Magazine

IEEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

Select Article Information

View: 1-25 | 26-50 | 51-75 |

- ☐ 1. **An iterative approach to hierarchical wire routing**
Etzel, A.;
Circuits and Systems, 1996. ISCAS '96., 'Connecting the World', 1996 IEEE International Symposium on
Volume 4, 12-15 May 1996 Page(s):663 - 666 vol.4
Digital Object Identifier 10.1109/ISCAS.1996.542111
[AbstractPlus](#) | Full Text: [PDF\(252 KB\)](#) IEEE CNF
- ☐ 2. **Back cover**
Proceedings of the IEEE
Volume 71, Issue 12, Dec. 1983 Page(s):c4 - c4
Full Text: [PDF\(3549 KB\)](#) IEEE JNL
- ☐ 3. **Four-bend top-down global routing**
Cho, J.D.; Sarrafzadeh, M.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction:
Volume 17, Issue 9, Sept. 1998 Page(s):793 - 802
Digital Object Identifier 10.1109/43.720316
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(364 KB\)](#) IEEE JNL
- ☐ 4. **A practical approach to the synthesis of arithmetic circuits using carry-si**
Taewhan Kim; Junhyung Um;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction:
Volume 19, Issue 5, May 2000 Page(s):615 - 624
Digital Object Identifier 10.1109/43.845087
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(288 KB\)](#) IEEE JNL
- ☐ 5. **Circuit layout**
Soukup, J.;
Proceedings of the IEEE
Volume 69, Issue 10, Oct. 1981 Page(s):1281 - 1304
[AbstractPlus](#) | Full Text: [PDF\(4103 KB\)](#) IEEE JNL
- ☐ 6. **VLSI: Technology and design**
Sarma, D.;
Proceedings of the IEEE
Volume 75, Issue 6, June 1987 Page(s):861 - 862
[AbstractPlus](#) | Full Text: [PDF\(270 KB\)](#) IEEE JNL
- ☐ 7. **CAD systems for VLSI in Japan**

Sudo, T.; Ohtsuki, T.; Goto, S.;
Proceedings of the IEEE
Volume 71, Issue 1, Jan. 1983 Page(s):129 - 143
[AbstractPlus](#) | Full Text: [PDF](#)(1878 KB) IEEE JNL

- ☐ **8. Automatic placement and routing techniques for gate array and standard**
Brady, H.N.; Blanks, J.;
Proceedings of the IEEE
Volume 75, Issue 6, June 1987 Page(s):797 - 806
[AbstractPlus](#) | Full Text: [PDF](#)(1015 KB) IEEE JNL
- ☐ **9. Scanning the issue**
Folberth, O.G.;
Proceedings of the IEEE
Volume 71, Issue 1, Jan. 1983 Page(s):3 - 4
[AbstractPlus](#) | Full Text: [PDF](#)(237 KB) IEEE JNL
- ☐ **10. Packaging Trade-Offs for an LSI-oriented Very High-Speed Computer, the**
Chiba, T.; Masaki, A.; Furumaya, K.; Hososaka, S.;
Components, Hybrids, and Manufacturing Technology, IEEE Transactions on |
Trans. on Components, Packaging, and Manufacturing Technology, Part A, B,
Volume 4, Issue 2, Jun 1981 Page(s):166 - 172
[AbstractPlus](#) | Full Text: [PDF](#)(1232 KB) IEEE JNL
- ☐ **11. Generalized Manhattan path algorithm with applications**
Asano, T.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction
Volume 7, Issue 7, July 1988 Page(s):797 - 804
Digital Object Identifier 10.1109/43.3950
[AbstractPlus](#) | Full Text: [PDF](#)(676 KB) IEEE JNL
- ☐ **12. A hexagonal array machine for multilayer wire routing**
Venkateswaran, R.; Maxumder, P.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction
Volume 9, Issue 10, Oct. 1990 Page(s):1096 - 1112
Digital Object Identifier 10.1109/43.62734
[AbstractPlus](#) | Full Text: [PDF](#)(1364 KB) IEEE JNL
- ☐ **13. Cross point assignment with global rerouting for general-architecture de**
Wen-Chung Kao; Tai-Ming Parng;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction
Volume 14, Issue 3, March 1995 Page(s):337 - 348
Digital Object Identifier 10.1109/43.365124
[AbstractPlus](#) | Full Text: [PDF](#)(1036 KB) IEEE JNL
- ☐ **14. Terrain based routing of distribution cables**
West, N.A.; Dwolatzky, B.; Meyer, A.S.;
Computer Applications in Power, IEEE
Volume 10, Issue 1, Jan. 1997 Page(s):42 - 46
Digital Object Identifier 10.1109/67.560861
[AbstractPlus](#) | Full Text: [PDF](#)(1156 KB) IEEE JNL
- ☐ **15. Logic emulation with virtual wires**
Babb, J.; Tessier, R.; Dahl, M.; Hanono, S.Z.; Hoki, D.M.; Agarwal, A.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction
Volume 16, Issue 6, June 1997 Page(s):609 - 626
Digital Object Identifier 10.1109/43.640619
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(520 KB) IEEE JNL
- ☐ **16. Automated evaluation of critical features in VLSI layouts based on photo simulations**

Sengupta, C.; Cavallaro, J.R.; Wilson, W.L., Jr.; Tittel, F.K.;

Semiconductor Manufacturing, IEEE Transactions on

Volume 10, Issue 4, Nov. 1997 Page(s):482 - 494

Digital Object Identifier 10.1109/66.641490

[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(1040 KB) IEEE JNL

- ☐ **17. Clock skew reduction in ASIC logic design: a methodology for clock tree**
Balboni, A.; Costi, C.; Pellencin, M.; Quadrini, A.; Sciuto, D.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction
Volume 17, Issue 4, April 1998 Page(s):344 - 356
Digital Object Identifier 10.1109/43.703824
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(340 KB) IEEE JNL
- ☐ **18. An efficient approach to multilayer layer assignment with an application minimization**
Chin-Chih Chang; Cong, J.J.S.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction
Volume 18, Issue 5, May 1999 Page(s):608 - 620
Digital Object Identifier 10.1109/43.759077
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(468 KB) IEEE JNL
- ☐ **19. Device-level early floorplanning algorithms for RF circuits**
Aktuna, M.; Rutenbar, R.A.; Carley, L.R.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction
Volume 18, Issue 4, April 1999 Page(s):375 - 388
Digital Object Identifier 10.1109/43.752922
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(1120 KB) IEEE JNL
- ☐ **20. EDA in IBM: past, present, and future**
Darringer, J.; Davidson, E.; Hathaway, D.J.; Koenemann, B.; Lavin, M.; Morrel K.; Roesner, W.; Schanzenbach, E.; Tellez, G.; Trevillyan, L.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction
Volume 19, Issue 12, Dec. 2000 Page(s):1476 - 1497
Digital Object Identifier 10.1109/43.898827
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(320 KB) IEEE JNL
- ☐ **21. Designing electronic engines with electronic engines: 40 years of bootstrap technology upon itself**
Jess, J.A.G.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction
Volume 19, Issue 12, Dec. 2000 Page(s):1404 - 1427
Digital Object Identifier 10.1109/43.898824
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(280 KB) IEEE JNL
- ☐ **22. Heterogeneous architecture models for interconnect-motivated system d**
Sek Meng Chai; Taha, T.M.; Wills, D.S.; Meindl, J.D.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 8, Issue 6, Dec. 2000 Page(s):660 - 670
Digital Object Identifier 10.1109/92.902260
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(412 KB) IEEE JNL
- ☐ **23. Wiring space and length estimation in two-dimensional arrays**
Jun Dong Cho;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction
Volume 19, Issue 5, May 2000 Page(s):612 - 615
Digital Object Identifier 10.1109/43.845086
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(156 KB) IEEE JNL
- ☐ **24. DUNE-a multilayer gridless routing system**
Cong, J.; Jie Fang; Kei-Yong Khoo;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction
Volume 20, Issue 5, May 2001 Page(s):633 - 647

Digital Object Identifier 10.1109/43.920694

[AbstractPlus](#) | [References](#) | Full Text: [PDF\(444 KB\)](#) IEEE JNL**25. Computer-aided design for large-scale integration**

Mays, C.;

Solid-State Circuits Conference. Digest of Technical Papers. 1967 IEEE Intern;
Volume X, Feb 1967 Page(s):46 - 47[AbstractPlus](#) | Full Text: [PDF\(208 KB\)](#) IEEE CNFView: [1-25](#) | [26-50](#) | [51-75](#) |

Indexed by

[Help](#) [Contact Us](#) [Privacy &](#)

© Copyright 2005 IEEE –



wire routing cad

1951

- 2001

Search

 Adv
 Sci
 Sci

Scholar

Results 1 - 10 of about 2,480 for wire routing cad . (0.07 seconds)

VPR: A new packing, placement and routing tool for FPGA research

V Betz, J Rose - FPL, 1997 - eecg.toronto.edu

... [17] JS Rose, "Parallel Global Routing for Standard ... on CAD, May 1992, pp. ... [19] G. Lemieux, S. Brown, "A Detailed Router for Allocating Wire Segments in ...

Cited by 220 - View as HTML - Web Search - mountains.ece.umn.edu - ecs.umass.edu - ece.wisc.edu - all 9 versions »

An Iterative-Improvement Penalty-Function-Driven Wire Routing System

R Linsker - IBM Journal of Research and Development, 1984 - portal.acm.org

... 2 Frank Rubin, An iterative technique for printed wire routing, Proceedings of the 11th workshop on Design automation, p.308-313 ... Computer-Aided Design CAD-2, No ...

Cited by 18 - Web Search - portal.acm.org - domino.research.ibm.com

Wire Routing and Satisfiability Planning

E Erdem, V Lifschitz, MDF Wang - Computational Logic, 2000 - springerlink.com

... We present a new approach to wire routing that uses ... the algorithms implemented in the existing routing systems in ... in computer-aided design (CAD) software is ...

Cited by 16 - Web Search - cs.utexas.edu - kr.tuwien.ac.at - portal.acm.org - all 6 versions »

Global wiring on a wire routing machine

R Nair, SJ Hong, S Liles, R Villani - Proceedings of the 19th conference on Design automation, 1982 - portal.acm.org

Page 1. GLOBAL WIRING ON A WIRE ROUTING MACHINE Ravi Nair, Se June Hong, Sandy Liles and Ray Villani IBM TJ Watson Research Center ...

Cited by 18 - Web Search - portal.acm.org

Channel density reduction by routing over the cells

MS Lin, HW Perng, CY Hwang, YL Lin - Proceedings of the 28th conference on ACM/IEEE design ..., 1991 - portal.acm.org

... 1, No. 1, pp. 25-35, Jan. 1982. 5 M. Burstein and R. Pelavin, "Hierarchical Wire Routing," IEEE Trans. on CAD of ICAS, Vol. 2, No. 4, pp. 223-234, Oct. 1983. ...

Cited by 16 - Web Search - portal.acm.org - ieeeexplore.ieee.org - csa.com - all 5 versions »

A detailed routing algorithm for allocating wire segments in field-programmable gate arrays

GG Lemieux, SD Brown - Proc. ACM/SIGDA Physical Design Workshop, Lake Arrowhead, CA ..., 1993 - ece.ubc.ca

... routing, the final stage in the CAD process, and ... that are most important with segmented routing channels, namely ... must be routed, that long wire segments should ...

Cited by 28 - View as HTML - Web Search - ece.ubc.ca - eecg.toronto.edu

New Performance Driven Routing Techniques With Explicit Area/Delay Tradeoff and Simultaneous Wire ...

J Lillis, CK Cheng, TTY Lin, CY Ho - DAC, 1996 - portal.acm.org

... New Performance Driven Routing Techniques With Explicit Area/Delay Tradeoff and Simultaneous Wire Sizing John Lillis, Chung-Kuan Cheng ...

Cited by 59 - Web Search - sigda.org - cs.ucsd.edu - ieeeexplore.ieee.org - all 8 versions »

DUNE: a multi-layer gridless routing system with wire planning

J Cong, J Fang, KY Khoo - ISPD, 2000 - portal.acm.org

... including wire sizing (for delay optimization), wire spacing (for ... l(a). In global routing, the routing region is ... author was with UCLA VLSI CAD Lab Permission ...

Cited by 24 - Web Search - cadlab.cs.ucla.edu - cadlab.cs.ucla.edu - portal.acm.org

REAL: a program for REGISTER ALLOCATION

FJ Kurdahi, AC Parker - Proceedings of the 24th ACM/IEEE conference on Design ..., 1987 - portal.acm.org
... 4 Akihiro Hashimoto, James Stevens, **Wire routing** by optimizing channel assignment within large apertures, Proceedings of the 8th ... [EEE Trans, on **CAD**, **CAD-5**(3 ...
[Cited by 103](#) - [Web Search](#) - portal.acm.org

Chameleon: a new multi-layer channel router

D Braun, J Burns, S Davadas, HK Ma, K Mayaram, F ... - Proceedings of the 23rd ACM/IEEE conference on Design ..., 1986 - portal.acm.org
... Ha71 Akihiro Hashimoto, James Stevens, **Wire routing** by optimizing ... Ha85 SE Hambruch, "Channel **Routing** Algorithms for Overlap Models ... **CAD** of ICs and Systems, vol ...
[Cited by 16](#) - [Web Search](#) - portal.acm.org

Goooooooooooooogle ►

Result Page: [1](#) [2](#) [3](#) [4](#) [5](#) [6](#) [7](#) [8](#) [9](#) [10](#) **[Next](#)**[Google Home](#) - [About Google](#) - [About Google Scholar](#)

©2005 Google



wire routing cad clamp

1951

- 2001

Search

Ad
Sch
Sch

Scholar

Results 1 - 10 of about 29 for wire routing cad clamp. (0.06 seconds)

WIRE BONDING DUAL-SIDED MCM-L MODULES

H Anderson, M Inc - Multichip Modules, 1994. Proceedings of the 1994 ..., 1994 - ieeexplore.ieee.org
 ... of heat to ambient - Mechanical housing - **CAD** system and ... PWB technology offers low
 cost, fair **routing** density (100 ... role in the success of the **wire** bond process ...
[Web Search](#) - ieeexplore.ieee.org - adsabs.harvard.edu

Application-Specific Integrated Circuits

MJS Smith, J Sebastian - 1997 - www-ee.eng.hawaii.edu
 ... 7.1 Actel ACT 275 7.1.1 **Routing** Resources 276 7.1.2 ... 2 Verilog Data Types 483
 11.2.3 Other **Wire** Types 486 11.2 ... 15.1 Physical Design 805 15.2 **CAD** Tools 807 15.2. ...
[Cited by 99](#) - [Cached](#) - [Web Search](#) - ce.aku.ac.ir - ce.aut.ac.ir - portal.acm.org - [all 7 versions »](#)

Package Clock Distribution Design Optimization for High-Speed and Low-Power VLSI's

Q Zhu, S Tam - IEEE Trans. Comp. Pack. Manuf. Technology, 1997 - ieeexplore.ieee.org
 ... [13] NC Chou and CK Cheng, "**Wire** length and ... [29] S. Tam, "Package clock **routing**
 feasibility study ... he was a R&D Team Leader of a national VLSI-**CAD** project in ...
[Cited by 11](#) - [Web Search](#) - ieeexplore.ieee.org

Design and implementation of a low-power clock-powered microprocessor

W Athas, N Tzartzanis, W Mao, L Peterson, R Lal, K ... - IEEE Journal of Solid-State Circuits, 2000 -
ieeexplore.ieee.org
 ... of the three metal layers are available for signal **routing**. ... The general **CAD** strategy
 was to design custom macros ... the 150-fF capacitance models a **wire** that is ...
[Cited by 12](#) - [Web Search](#) - hwswworld.com - ieeexplore.ieee.org - csa.com

A Web-based Framework for Design and Manufacturing a Mechanical System

MJ Chung, P Kwon - DETC, Atlanta, Georgia. Sep, 1998 - edge.mcs.drexel.edu
 ... Such tool provides a means (1) to integrate many specialized tools such as **CAD** and
 FEM packages, (2) to assist designers to ... Global **Routing** ... **Wire** Assignment ...
[Cited by 2](#) - [View as HTML](#) - [Web Search](#)

What is the cost of delay insensitivity?

H Saito, A Kondratyev, J Cortadella, L Lavagno, A ... - IEEE ACM INT CONF COMPUT AIDED DES DIG TECH
 PAP. pp. 316-323 ..., 1999 - doi.ieeeecomputersociety.org
 ... by the tool Petrify [3]. Asynchronous **CAD** is being ... example in Figure 1). In particular,
routing can be ... arbitrary delays to every input **wire** may unpredictably ...
[Cited by 5](#) - portal.acm.org - sigda.org - lsi.upc.es - [all 12 versions »](#)

Bounds on net lengths for high-speed PCBs.

J Lee, E Shragowitz, D Poli - 1993 - ieeexplore.ieee.org
 ... **Routing** of the large board may take many hours on ... Layout constraints are the maximal
wire length allowed between a ... high level is 2 volt and **clamp** diodes were ...
[Cited by 3](#) - [Web Search](#) - portal.acm.org - portal.acm.org - csa.com - [all 5 versions »](#)

An embedded 32-b microprocessor core for low-power and high-performance applications

LT Clark, EJ Hoffman, J Miller, M Biyani, Y Liao, ... - IEEE Journal of Solid-State Circuits, 2001 -
ieeexplore.ieee.org
 ... line capacitance, as well as increased **routing** tracks for ... A combination of inline
 and staggered **wire** bondpads were ... speed digital datapath design, and IC **CAD/CAE** ...
[Cited by 47](#) - [Web Search](#) - ee.princeton.edu - ce.chalmers.se - eecs.harvard.edu - [all 8 versions »](#)

Electrical characteristics of interconnections for high-performance systems

A Deutsch - Proceedings of the IEEE, 1998 - ieeexplore.ieee.org
... cross sec- tions caused by discontinuities such as connectors, vias, **wire** bonds, flip ... An active **clamp** network, such as one using Schottky barrier diodes [16 ...
[Cited by 42](#) - [Web Search](#) - ida.ing.tu-bs.de - ieeexplore.ieee.org

Bitwidth analysis with application to silicon compilation

M Stephenson, J Babb, S Amarasinghe - PLDI, 2000 - portal.acm.org
Page 1. Bitwidth Analysis with Application to Silicon Compilation Mark Stephenson, Jonathan Babb, and Saman Amarasinghe Massachusetts ...
[Cited by 99](#) - [Web Search](#) - lcs.mit.edu - portal.acm.org - csa.com

Google ►

Result Page: 1 2 3 **Next** :

[Google Home](#) - [About Google](#) - [About Google Scholar](#)

©2005 Google



wire routing cad fastener

1951

- 2001

Search

Adv
Sci
Sch

Scholar

Results 1 - 9 of 9 for wire routing cad fastener. (0.08 seconds)

The design and planning of cable harness assemblies

FM Ng, JM Ritchie, JEL Simmons - Proceedings of the Institution of Mechanical Engineers. Pt. ..., 2000 - ingentaconnect.com

... such as duplicated pins and connector **wire** gauge mis ... of the circuits and may require the re-**routing** of the ... were then manually entered into their **CAD** systems to ...

Cited by 6 - Web Search - ingentaconnect.com - csa.com - csa.com

Positioning and Orienting a Drill Axis on a Curved Surface

PG Iovenitti, E Mutapcic, CR Nagarajah - The International Journal of Advanced Manufacturing ..., 2001 - springerlink.com

... the 3D coordinate data to the **CAD** model, and ... of applications including drilling, **routing**, water jet ... arc welding, composites fabrication, **wire** harness fabrication ...

Web Search - csa.com

Influence of computer chassis design on metal fabrication waste streams

P Sheng, B Willis, A Shiovitz - The 1995 IEEE International Symposium on Electronics and the ..., 1995 - ieeexplore.ieee.org

... Figure 2). Specific parts may have different **routing** due to ... safety and minimize the risk of **wire** short-circuit. ... The vendor receives 3-D **CAD** data from the ...

Web Search - ieeexplore.ieee.org - csa.com

Section A

B Section - Signature, 1998 - gsp.extra.daimlerchrysler.com

... They shall produce assemblies in accordance wit models, **cad** information or approved ...

Assembly on Floor 60% Mechanical Complete 80% Pipe and **Wire** Complete (pipe ...

View as HTML - Web Search - 212.67.202.176 - cache.org.uk - channel4.com - all 508 versions »

[book] Fundamentals of Robotics

DD Ardayfio - 1987 - print.google.com

... **CAD/CAM** Systems Planning and Implementation, by Charles S. Knox 23. ... Engineering Documentation for **CAD/CAM** Applications, by Charles S. Knox 31. ...

Cited by 4 - Web Search - Library Search

[book] Understanding the Manufacturing Process

J Harrington Jr - 1984 - print.google.com

... of Limit Analysis, Betzalel A vitzur 5. Improving Productivity by Classification, Coding, and Data Base Standardization : The Key to Maximizing **CAD/CAM** and ...

Cited by 13 - Web Search

[PS] Supporting collaborative design by embedding communication and history in design artifacts

BN Reeves - 1993 - twinbear.com

Page 1. Supporting Collaborative Design by Embedding Communication and History in Design Artifacts by Brent Neal Reeves BBA, Abilene Christian University, 1980 ...

Cited by 18 - View as HTML - Web Search - srainc.com - cs.colorado.edu - portal.acm.org - all 6 versions »

[book] A Mathematical Theory of Design: Foundations, Algorithms, and Applications

D Braha, O Maimon - 1998 - print.google.com

... 612 Chapter 10.3) 20.5 **Fastener** Design Example 614 ... 614 20.5.2 The Production Rules 615 20.5.3 **Fastener** Synthesis Using the Design Search Algorithm 620 ...

Cited by 19 - Web Search - Library Search

2000

ADS Compendium - London: Datapharma Publications Ltd, 2000 - mmo.on.ca

... 43 Optimal Surface Quality of **Wire** Rod Gary Purdy, McMaster University 43 ...

[Cited by 2](#) - [View as HTML](#) - [Web Search](#)

wire routing cad fastener

Search

[Google Home](#) - [About Google](#) - [About Google Scholar](#)

©2005 Google

[Adv](#)
[Sci](#)
[Sch](#)**Scholar**Results 1 - 1 of 1 for **wire routing cae fastener**. (0.07 seconds)

[book] [A Mathematical Theory of Design: Foundations, Algorithms, and Applications](#)

D Braha, O Maimon - 1998 - [print.google.com](#)

... 612 Chapter 10.3) 20.5 **Fastener** Design Example 614 ... 614 20.5.2 The Production Rules

615 20.5.3 **Fastener** Synthesis Using the Design Search Algorithm 620 ...

Cited by 19 - [Web Search](#) - [Library Search](#)

[Google Home](#) - [About Google](#) - [About Google Scholar](#)

©2005 Google



cable routing cad clamp

1951

- 2001

Search

Adv
Sch
Sch**Scholar**Results 1 - 10 of about 11 for **cable routing cad clamp**. (0.08 seconds)Section A

B Section - Signature, 1998 - gsp.extra.daimlerchrysler.com

... mats, emergency stop push-buttons, cycle stop push-buttons, cycle start push-buttons, **cable** tray and ... System/equipment installation layout **CAD** drawings (ie. ...[View as HTML](#) - [Web Search](#) - 212.67.202.176 - [cache.org.uk](#) - [channel4.com](#) - all 508 versions »[book] Cables and Wiring

J Cadick, MA Avo - 1998 - print.google.com

... xi PART ONE Covers general wire and **cable** theory, as well as **cable** materials and construction, installation, splicing, termination, and testing procedures. ...[Web Search](#) - [Library Search](#)[book] Plastics Engineering, Manufacturing & Data Handbook

DV Rosato - 2001 - print.google.com

... IM Techniques, IM Continuously, Electrical Insulates Buttons for Coaxial **Cable** ... Thread Tapping 494; Sawing, Milling, Thinning, Grinding, **Routing** 494; Machining ...[Web Search](#) - [Library Search](#)A Monolithic Switching Regulator with 100 μ V Output Noise

J Williams - Linear Technology Corporation, Application Note, 1997 - linear.com

... BNC **CABLE** AN70 F08 BNC **CABLE** AND CONNECTORS ... All you **CAD** modeling types out there might want to think about that. Note 11: See Figure 3's Block Diagram. ...Cited by 10 - [View as HTML](#) - [Web Search](#) - [linear.com.cn](#)[book] Network Design: Management and Technical Perspectives

TC Mann-Rubinson, K Terplan - 1998 - print.google.com

Page 1. NETAORK DESIGN ManagementandTechnicalPerspecfives TeresaC.Mann-Rubinson

KornelTerplan CRC Press Boca Raton London New York Washington, DC Th isOn ...

Cited by 4 - [Web Search](#)Electrical characteristics of interconnections for high-performance systems

A Deutsch - Proceedings of the IEEE, 1998 - ieeexplore.ieee.org

... This **clamp** should be designed to have an equivalent impedance matched to the line ... a given interconnect used in digital systems such as on a **cable**, for example. ...Cited by 42 - [Web Search](#) - [ida.ing.tu-bs.de](#) - [ieeexplore.ieee.org](#)[book] Fundamentals of Robotics

DD Ardayfio - 1987 - print.google.com

... **CAD/CAM** Systems Planning and Implementation, by Charles S. Knox 23. ... Engineering Documentation for **CAD/CAM** Applications, by Charles S. Knox 31. ...Cited by 4 - [Web Search](#) - [Library Search](#)[book] Progress in Robotics and Intelligent Systems

GW Zobrist - 1994 - print.google.com

Page 1. PROGRESS in ROBOTICS and INTELLIGENT SYSTEMS VOLUME I edited by George W. Zobrist and CY (Pete) Ho University of Missouri Rolla ...

[Web Search](#)[book] Pultrusion for Engineers

T Starr, T Starr, TF Starr, J Ketel, D Shaw- ... - 2000 - print.google.com

Page 1. Pultrusion for engineers Th isOn Page 2. Pultrusion for engineers Edited by Trevor F Starr CRC Press Boca Raton Boston New York Washington, DC ...

[Cited by 1](#) - [Web Search](#) - [woodhead-publishing.com](#) - [Library Search](#)

Template modified: 27 May 1997 14: 30

PAIRF COMMANDER, P INSTRUCTION, PPIN AIRCRAFT - Personnel, 1994 - e-publishing.af.mil

... 2.6.4.4.3. Maintain currency in all aspects of life support and SERE training

and use of appli- **cable** life support equipment. 2.6 ...

[View as HTML](#) - [Web Search](#) - [e-publishing.af.mil](#)

Google ►

Result Page: 1 2 [Next](#)

[Google Home](#) - [About Google](#) - [About Google Scholar](#)

©2005 Google



cable routing cad fastener

1951

- 2001

Search

Ad
Sch
Sch

Scholar

Results 1 - 7 of 7 for **cable routing cad fastener**. (0.06 seconds)The design and planning of **cable** harness assemblies

FM Ng, JM Ritchie, JEL Simmons - Proceedings of the Institution of Mechanical Engineers. Pt. ..., 2000 - ingentaconnect.com

... Three-dimensional **CAD** THE DESIGN AND PLANNING OF **CABLE** HARNESS ASSEMBLIES ... design software and wiring lists are used as inputs for the harness **routing** package. ...Cited by 6 - [Web Search](#) - [ingentaconnect.com](#) - [csa.com](#) - [csa.com](#)The scanning mechanism for Rosetta/MIDAS from an engineering model to the flight model

R Le Letty, F Barillot, N Lhermet, F Claeysen, M ... - ESA SP, 2001 - cedrat.com

... latch status indicator, 10 : washer, 11 : **fastener** return spring ... to include this aspect into the **CAD** model to ... Figure 21 : View of the **cable's routing** on the FM ...Cited by 3 - [View as HTML](#) - [Web Search](#) - [cedrat-grenoble.fr](#) - [adsabs.harvard.edu](#) - [csa.com](#) - [all 5 versions »](#)Section A

B Section - Signature, 1998 - gsp.extra.daimlerchrysler.com

... mats, emergency stop push-buttons, cycle stop push-buttons, cycle start push-buttons, **cable** tray and ... System/equipment installation layout **CAD** drawings (ie. ...[View as HTML](#) - [Web Search](#) - [212.67.202.176](#) - [cache.org.uk](#) - [channel4.com](#) - [all 508 versions »](#)[PS] Supporting collaborative design by embedding communication and history in design artifacts

BN Reeves - 1993 - twinbear.com

Page 1. Supporting Collaborative Design by Embedding Communication and History in Design Artifacts by Brent Neal Reeves BBA, Abilene Christian University, 1980 ...

Cited by 18 - [View as HTML](#) - [Web Search](#) - [srainc.com](#) - [cs.colorado.edu](#) - [portal.acm.org](#) - [all 6 versions »](#)[book] Fundamentals of Robotics

DD Ardayfio - 1987 - print.google.com

... **CAD/CAM** Systems Planning and Implementation, by Charles S. Knox 23. ... Engineering Documentation for **CAD/CAM** Applications, by Charles S. Knox 31Cited by 4 - [Web Search](#) - [Library Search](#)[book] Understanding the Manufacturing Process

J Harrington Jr - 1984 - print.google.com

... of Limit Analysis, Betzalel A vitzur 5. Improving Productivity by Classification, Coding, and Data Base Standardization : The Key to Maximizing **CAD/CAM** and ...Cited by 13 - [Web Search](#)Template modified: 27 May 1997 14: 30

PAIRF COMMANDER, P INSTRUCTION, PPIN AIRCRAFT - Personnel, 1994 - e-publishing.af.mil

... 2.6.4.4.3. Maintain currency in all aspects of life support and SERE training and use of appli- **cable** life support equipment. 2.6 ...[View as HTML](#) - [Web Search](#) - [e-publishing.af.mil](#)

cable routing cad fastener

Search

[Google Home](#) - [About Google](#) - [About Google Scholar](#)

©2005 Google

Adv
Sch
Sch**Scholar**

Results 1 - 2 of 2 for cable routing cae clamp. (0.05 seconds)

[book] Plastics Engineering, Manufacturing & Data Handbook

DV Rosato - 2001 - print.google.com

... Continuously, Electrical Insulates Buttons for Coaxial **Cable** ... Machine Set- tings from**CAE** Analysis Result ... Milling, Thrn- ing, Grinding, **Routing** 494; Machining ...[Web Search](#) - [Library Search](#)**Alternative Cover Assessment Program: Phase II Report**

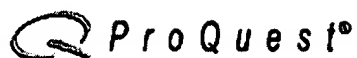
M Bolen, A Roesler, C Benson, W Albright - Geo Engineering Rep. No, 2001 - uwgeotech.org

Page 1. Alternative Cover Assessment Program: Phase II Report By Michael

M. Bolen Science Applications International Corporation ...

Cited by 6 - [View as HTML](#) - [Web Search](#) - [acap.dri.edu](#) - [dri.edu](#) - [acap.dri.edu](#)[Google Home](#) - [About Google](#) - [About Google Scholar](#)

©2005 Google

[Return to the USPTO NPL Page](#) | [Help](#)

Basic

Advanced

Topics

Publications

My Research

0 marked items

Interface language:

English

[What's new](#)

Databases selected: Multiple databases...

Results – powered by ProQuest® Smart Search**Suggested Topics** [About](#)< Previous | [Next](#) >**Browse Suggested Publications**< Previous | [Next](#) >[Computer aided design](#)[Computer aided design AND Software](#)[Computer aided design AND Software packages](#)[Computer aided design AND Design engineering](#)[Design News; Boston](#)[Machine Design; Cleveland](#)[Mechanical Engineering; New York](#)2 documents found for: *TEXT(wire rout*) AND TEXT(cad) AND PDN(<8/9/2001)*[Set up Alert](#)[About](#)☐ Mark
all 0 marked items: Email / Cite /
Export Show all
documentsSort results by: [Most recent first](#)

- ☐ 1. **A comparison of pin actuation schemes for large-scale discrete dies**
Yong-Tai Im, Daniel F Walczyk, Robert C Schwarz, John M Papazian. Journal of Manufacturing Processes. Dearborn: 2000. Vol. 2, Iss. 4; p. 247 (11 pages)

[Text+Graphics](#) [Page Image - PDF](#) [Abstract](#)

- ☐ 2. **Discrete Wiring: A Systems Approach To High Speed Design Problems**
Buck, T. J.. Circuit World. Bradford: 1997. Vol. 23, Iss. 1; p. 9

[Full text](#) [Abstract](#)

1-2 of 2

Want an alert for new results sent by email? [Set up Alert](#) [About](#)Results per page: [30](#)**Advanced Search**Tools: [Search Tips](#) [Browse Topics](#) [2 Recent Searches](#)

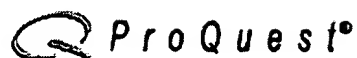
wire rout*	Document text
AND	cad
AND	
	Citation and abstract

[Add a row](#) | [Remove a row](#)[Search](#)[Clear](#)Database: [Multiple databases...](#) [Select multiple databases](#)Date range: [Before this date...](#) [08/09/2001](#) [About](#)Limit results to: ☒ Full text documents only ☒ Scholarly journals, including peer-reviewed [About](#)[More Search Options](#)

Copyright © 2005 ProQuest Information and Learning Company. All rights reserved. [Terms and Conditions](#)

[Text-only interface](#)



[Return to the USPTO NPL Page](#) | [Help](#)

Basic

Advanced

Topics

Publications

My Research
0 marked items

Interface language:

English

Databases selected: Multiple databases...

[What's new](#)

Searching for *TEXT(cable rout*) AND TEXT(cad) AND PDN(<8/9/2001)* did not find any documents. Try the following:

[Suggested Topics](#) [About](#)< Previous | [Next >](#)[Browse Suggested Publications](#)
[About](#)< Previous |
[Next >](#)[Computer aided design](#)[Computer aided design AND Software](#)[Computer aided design AND Software packages](#)[Computer aided design AND Autodesk Inc](#)[\(company/org\)](#)[Design News; Boston](#)[Machine Design; Cleveland](#)[Mechanical Engineering; New York](#)

-OR-

Revise your search below using the following tips:

- Check your spelling.
- Reduce the number of terms included in your search.
- Broaden your search by selecting other [databases](#), removing limits, or searching "Citations and Document Text" (if available).
- Use "AND" to connect two words that don't need to be searched as a phrase.
- Connect similar terms with the "OR" operator (e.g. military OR pentagon). See [Search Tips](#) for more hints.

Advanced Search

Tools: [Search Tips](#) [Browse Topics](#) [3 Recent Searches](#)

<input type="text" value="cable rout*"/>	<input type="text" value="Document text"/>
<input type="text" value="AND"/>	<input type="text" value="cad"/>
<input type="text" value="AND"/>	<input type="text" value="Citation and abstract"/>

[Add a row](#) | [Remove a row](#)

Database: [Select multiple databases](#)Date range: [About](#)Limit results to: ☒ Full text documents only ☒ Scholarly journals, including peer-reviewed [About](#)[More Search Options](#)Copyright © 2005 ProQuest Information and Learning Company. All rights reserved. [Terms and Conditions](#)[Text-only interface](#)

Searching for **wire routing and cad**.

Restrict to: [Header](#) [Title](#) Order by: [Expected citations](#) [Hubs](#) [Usage](#) [Date](#) Try: [Google \(CiteSeer\)](#) [Google \(Web\)](#) [Yahoo!](#) [MSN](#) [CSB](#) [DBLP](#)

24 documents found. Order: number of citations.

Chernoff-Hoeffding Bounds for Applications with Limited.. - Schmidt, Siegel.. (1993) (Correct) (44 citations)
for random sampling **and** oblivious packet **routing**. 1 Introduction The most fundamental tools used the tail probabilities of the sums of bounded **and** independent random variables. We present a simple cs.nyu.edu/cs/faculty/siegel/Limited.ps

The Post Office Experience: Designing a Large Asynchronous.. - Davis, Stevens, Coates (1993) (Correct) (43 citations)

circuitry takes up 45% pads cover 11% **wire routing** requires 19% and the other 6% is unused space and complex device would be well supported by our **CAD** capability. What follows is a brief description of synthesizing the AFSMs. Since we were not experienced **CAD** people, we grossly underestimated the need to pay www.cs.utah.edu/~ald/hicss.ps

Rectilinear Paths among Rectilinear Obstacles - Lee, Yang, Wong (1996) (Correct) (12 citations)
fields, such as motion planning in robotics, **wire routing** in VLSI and logistics in operations research. Computed-Aided Design for PCB or VLSI circuit **routing**, **wires** and modules are usually restricted to lie on Antognetti, A tile-expansion router, IEEE Trans. **CAD**, Vol. **CAD-6**, no.4, 1987, 507-517. 45] K. M. web.eecs.nwu.edu/~dtlee/Discretemath_survey.ps.Z

FPGA Routing Architecture: Segmentation and Buffering to.. - Betz, Rose (1999) (Correct) (8 citations)
routing architecture. Pass transistor Routing **wire routing** switch Tri-state buffer routing switch Logic defines such features as: 1. The length of each **routing wire** segment (how many logic blocks a **routing wire** less accurate, delay and area metrics. Third, the **CAD** flow we use to evaluate architectures employs a www.eecg.toronto.edu/~jayar/pubs/betz/fpga99betz.ps.gz

Physical Hierarchy Generation with Routing Congestion Control - Chang, Cong, Pan, Yuan (2002) (Correct) (5 citations)

bounding box wire length but 3 6% shorter **routing wire** length measured by graph based A-tree. Handling High Complexity Designs In The Vlsi **Cad** Area [16, 17, 18] The Backbone Of Our System Is A ballade.cs.ucla.edu/~cong/papers/p64-chang.pdf

Logic Synthesis for Cellular Architecture FPGA using BDD - Lee (1997) (Correct) (4 citations)
d) is not a Maitra term and it needs another **routing wire** to be realized in the cellular www.ee.pdx.edu/~mperkows/ps/lee-visitor-korea.ps

A Negative Reinforcement Method for PGA Routing - Lewis, Wang (1993) (Correct) (3 citations)
as well as leading to shorter overall **routing wire** length. This paper is organized as follows. Lewis and Wang 2 After the specification stage, the **CAD** process for FPGA's proceeds through logic Technique for Global Wiring. IEEE Trans. on **CAD**, vol. **CAD-6**, no. 2, March 1987, 165-172. NRT86 www.cs.engr.uky.edu/~lewis/papers/negative.pdf

Parallel Algorithms for VLSI Circuit Extraction - Belkhale, Banerjee (1991) (Correct) (3 citations)
circuit extraction, cell placement and **wire routing** will increase tremendously. There will be an Orders Of Magnitude Performance Improvements In Vlsi **Cad** Applications. In This Paper, We Propose Parallel the computational requirements of performing various **CAD** tasks such as simulation, design-rule checking, www.ece.nwu.edu/cpdc/ProperCAD/tcad91.bb.ps.Z

Mixing Buffers and Pass Transistors in FPGA Routing Architectures - Sheng, Rose (2001) (Correct) (2 citations)

of an FPGA consists of: 1. The length of each **routing wire** in the FPGA measured in terms of number of as follows: Section 2 outlines the experimental **CAD** flow which is used to profile the previous Figure 2 illustrates the empirical methodology and **CAD** flow used to evaluate routing architectures. It is www.eecg.toronto.edu/~jayar/pubs/sheng/shengfpga01.ps

Automated Detection of Pulmonary Nodules in Helical.. - Lee, Hara, Fujita.. (2001) (Correct) (2 citations)
applied to such optimization problems as **wire routing**, scheduling, adaptive control, game playing, to develop a technique for computer-aided diagnosis (**CAD**) systems to detect lung nodules in helical X-ray

that our scheme can be regarded as a technique for **CAD** systems to detect nodules in helical CT pulmonary
www.isi.uu.nl/Meetings/.../TGV/Lee01a.pdf

Parallel Algorithms For CAD With Applications To Circuit Extraction - Belkhale (1991) (Correct) (2 citations)
 circuit extraction, cell placement and **wire routing** will increase tremendously. There will be an
 Parallel Algorithms For **Cad** With Applications To Circuit Extraction By Krishna
 CHAPTER 1. INTRODUCTION 1.1. Parallel Processing for **CAD** As the sizes of VLSI circuits increases in the
www.ece.nwu.edu/cpdc/ProperCAD/phd90.b.ps.Z

Circuit Design of Routing Switches - Guy Lemieux University (2002) (Correct) (1 citation)
 each transistor in the cluster, including the **routing**. **Wire** RC values are determined from the tile size
 used for the HSPICE simulations in Section 3 and the **CAD** flow in the later sections. 2.1 HSPICE Circuit
 V. Betz, J. Rose, and A. Marquardt, Architecture and **CAD** for Deep-Submicron FPGAs. Boston: Kluwer
 Academic
www.eecg.toronto.edu/~lemieux/publications/FPGA02.ps.gz

Wire Routing and Satisfiability Planning - Erdem, Lifschitz, Wong (2000) (Correct) (1 citation)
Wire Routing and Satisfiability Planning Esra Erdem,
 research and development in computer-aided design (**CAD**) software is very active in both industry and
 and academia. Routing is an important step in **CAD** for VLSI circuits [7]It is the problem of
www.cs.utexas.edu/users/esra/papers/cl00.ps

More on Wire Routing with ASP - East, Truszczynski (2001) (Correct) (1 citation)
 More on **Wire Routing** with ASP Deborah East and Mirosław Truszczynski
 size of circuits, research in computer aided design (**CAD**) for VLSI is an active area of research. In a
www.cs.nmsu.edu/~tson/ASP2001/16.ps

ETDD-based Synthesis of Term-Based FPGAs for Incompletely.. - Lee, Drechsler (1998) (Correct) (1 citation)
 be implemented in a cell array without extra **routing wire**. Example 1 1. A logic expression (ab)cd can
www.informatik.uni-freiburg.de/~drechsle/ps_test/ETDDSYNTH.ps

Succinct Representation of Graphs - Project Report For (Correct)
 analysis)minimum spanning forest (used in **wire routing** and layout) are of interest. 3.1 Small
 The Primary Target For These Models Were Vlsi **Cad** Applications. In This Project We Show That One Of
 To Reduce The Space And Time Complexity Of Vlsi **Cad** Applications. Although Bdds Have Several Desirable
www.cs.utexas.edu/users/karu/docs/graphs.ps

Optimized Pin Assignment for Lower Routing Congestion - After Floorplanning Phase (Correct)
 optimization goal is generally to reduce the **routing wire** length and/or the circuit area. Permission to
www.cs.ucla.edu/~mrivero/PAPER/p17-zhang.pdf

Concurrent Product Design: A Case Study On The Pico Radio Test.. - Odell, Wright (2002) (Correct)
 gap around the PCB stack to allow for **wire routing** and antenna placement. Four long screw bosses
 access to the board stack components. **Wire Routing** **Wire routing** is often an overlooked aspect in
 o Tes Bed Cas ing Cover Serial Port Window Figure 2: **CAD** model of PRTB version 1 assembly 3 Copyright
everandever.com/dan/publications/DETC2002_DFM-34154.pdf

Unknown - (Correct)
 wiring rule checking, component placement and **wire routing**. Computers have been used to a lesser extent
www.lcs.mit.edu/publications/pubs/ps/tr-31.ps

First 20 documents [Next 20](#)

Try your query at: [Google \(CiteSeer\)](#) [Google \(Web\)](#) [Yahoo!](#) [MSN](#) [CSB](#) [DBLP](#)

CiteSeer.IST - Copyright [Penn State](#) and [NEC](#)